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GB 2209858 A EP 0424191 A2 EP 0198935 A1
WO 84/01236 A1 US 4817056 A US 4532611 A

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(54) Row redundancy for flash memories

(57) A method and apparatus for providing row redundancy in EEPROM's provides for preconditioning of each row of memory cells prior to erasing the memory array, including any rows containing defective cells as well as any redundant rows. If a first row is addressed for a read operation and if the first row is not functioning properly, the third word line is selected. If the second row is addressed for a read operation and if the second row is not functioning properly, the fourth word line is selected. Alternatively if the first row is addressed and if the first row is not functioning properly the second word line is selected. An alternate word line in redundant rows 48 may be selected by setting the address of a shorted word line in one of the content addressable memories CAMS 46.

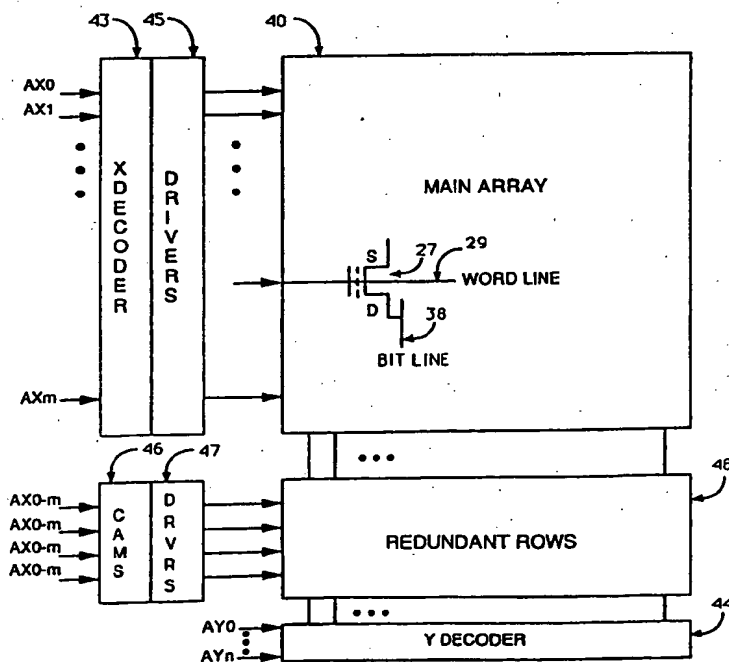


FIGURE 3

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

FIGURE 1 (PRIOR ART)

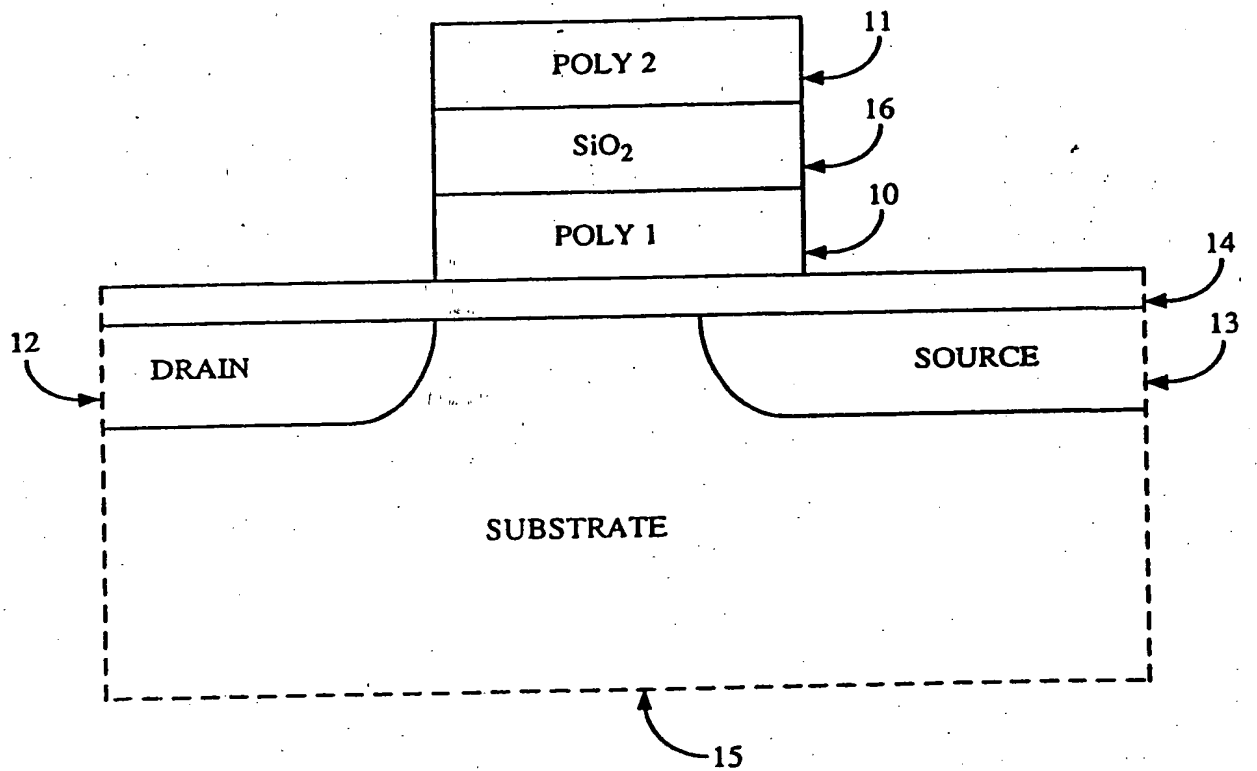


FIGURE 2 (PRIOR ART)

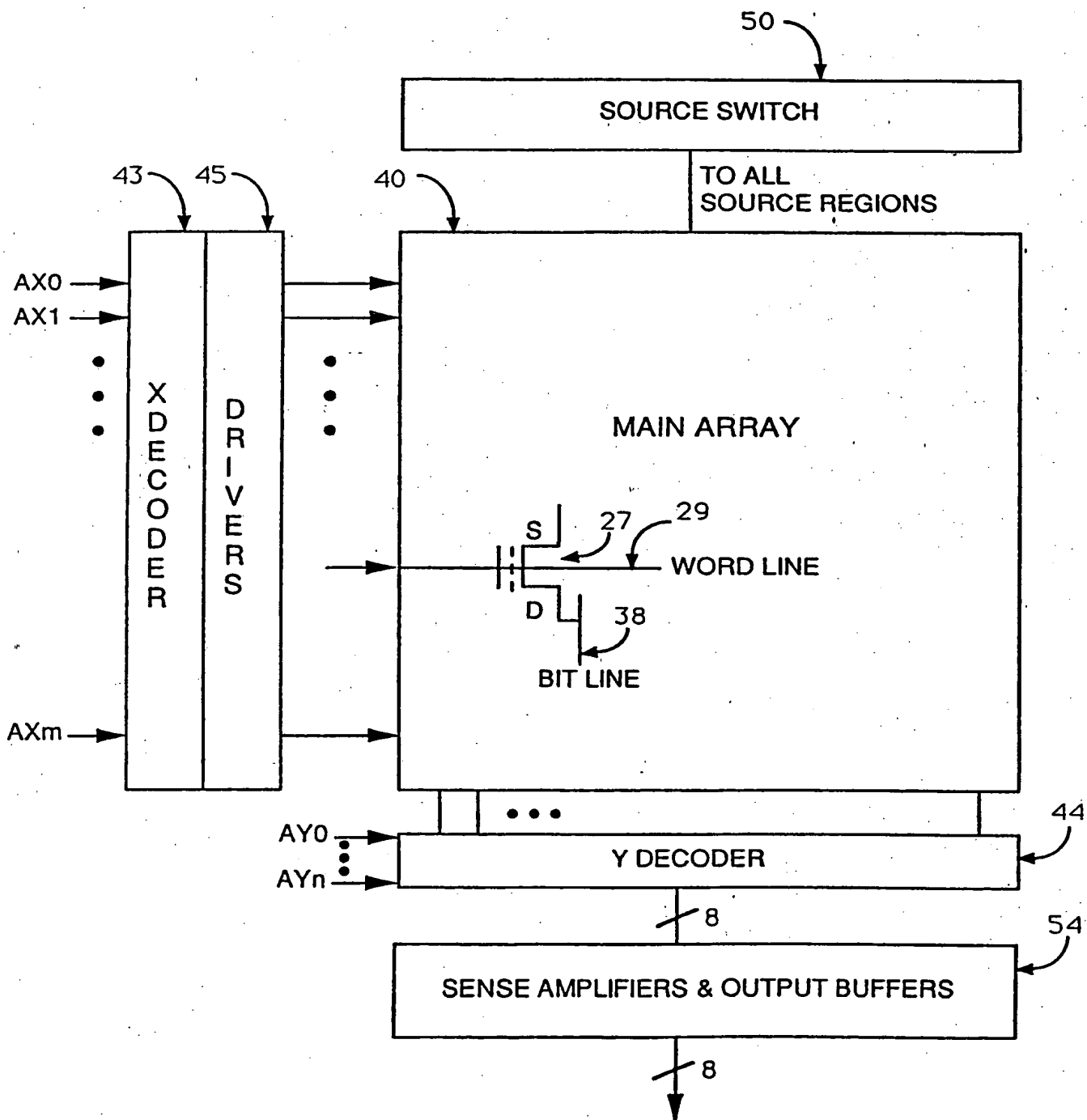
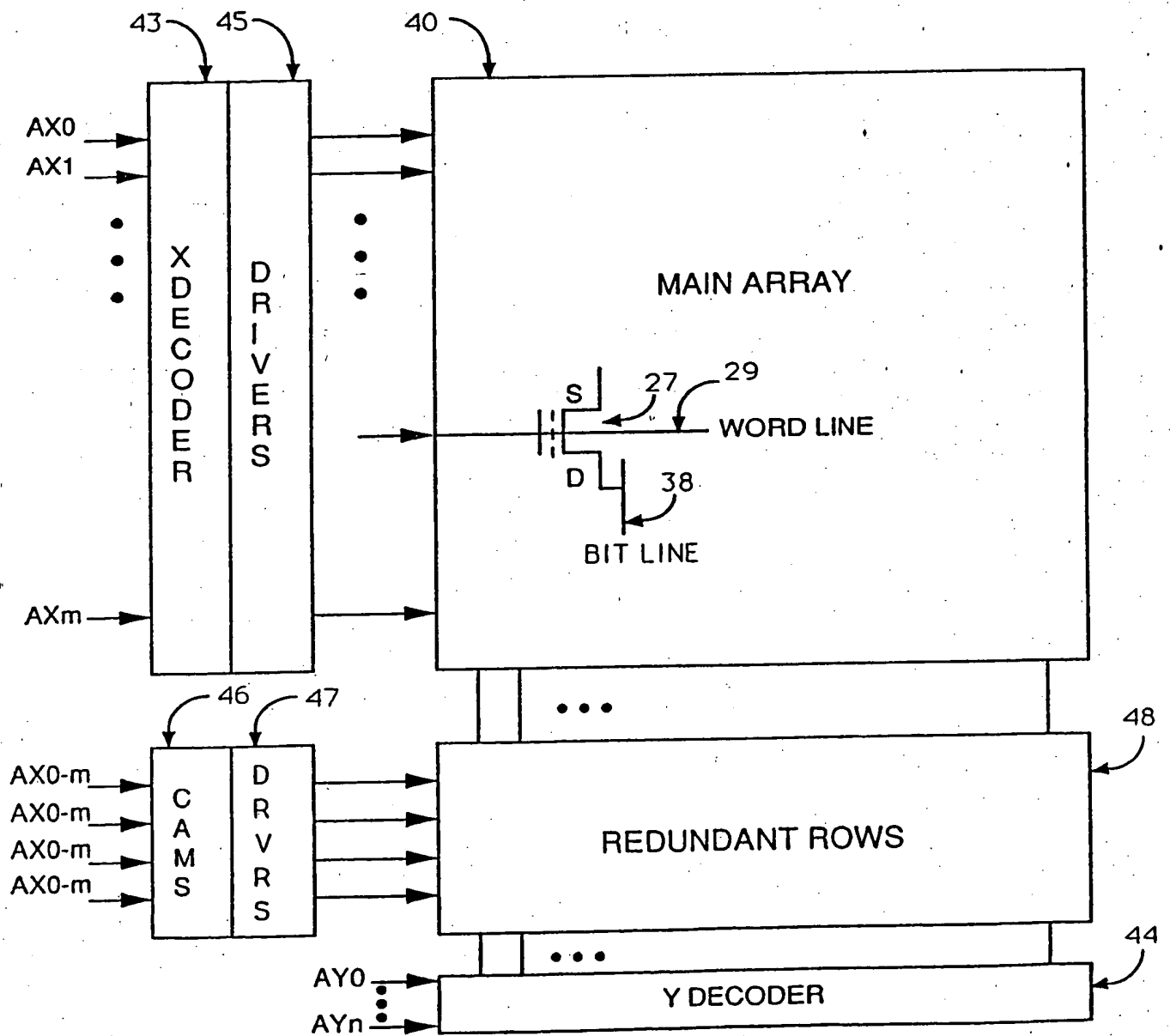


FIGURE 3



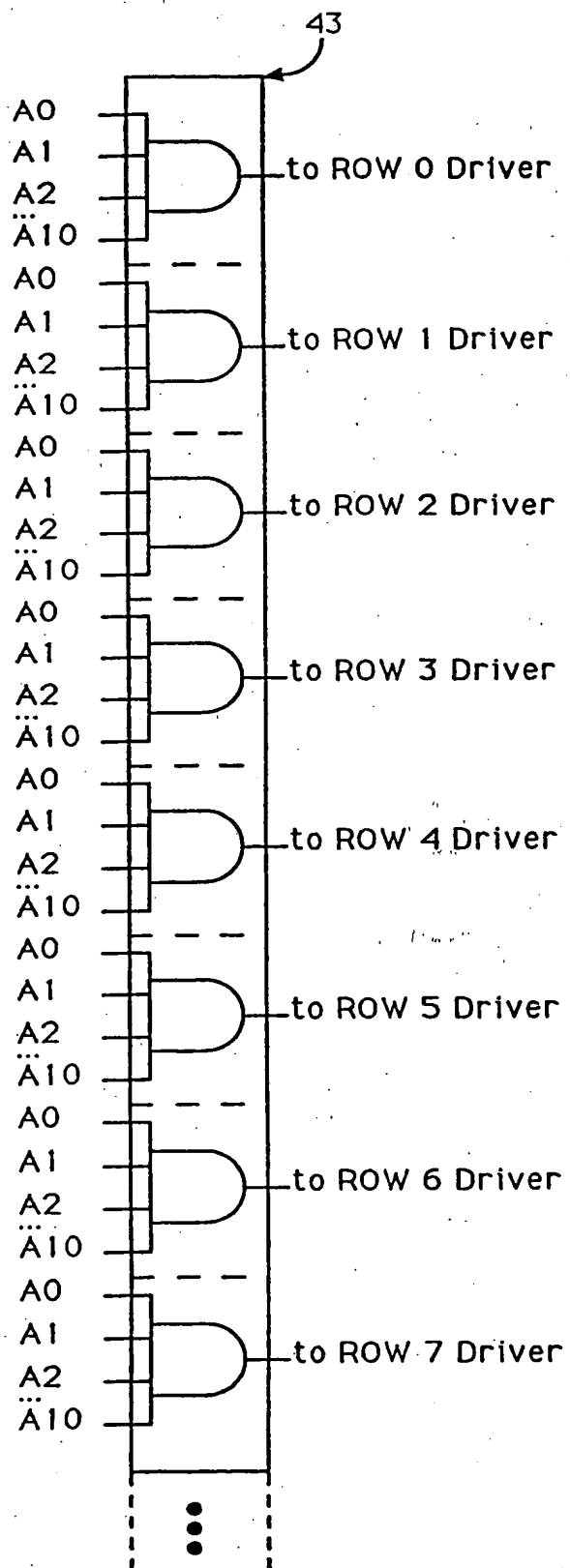


FIGURE 4 (PRIOR ART)

FIGURE 5 (PRIOR ART)

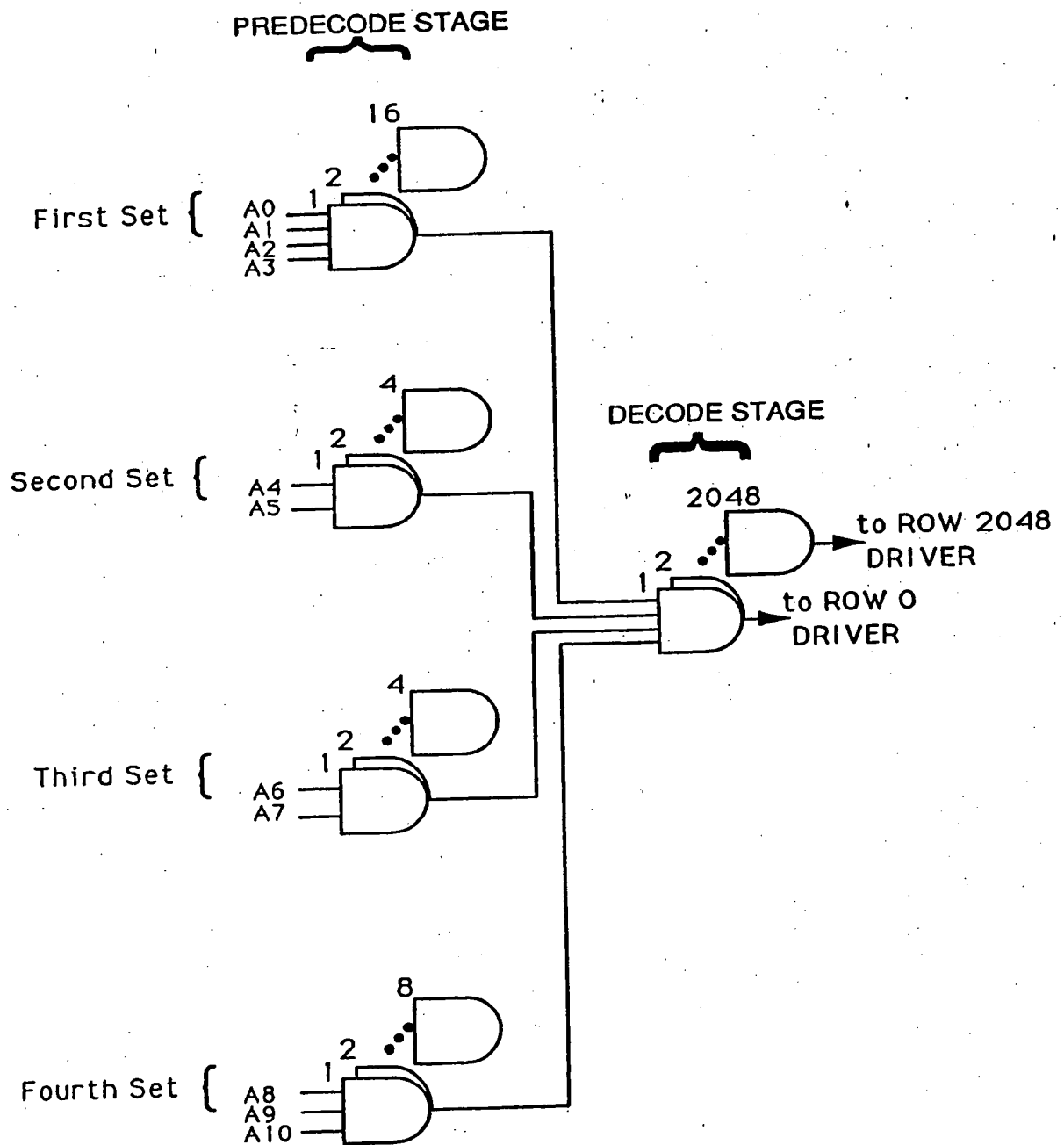
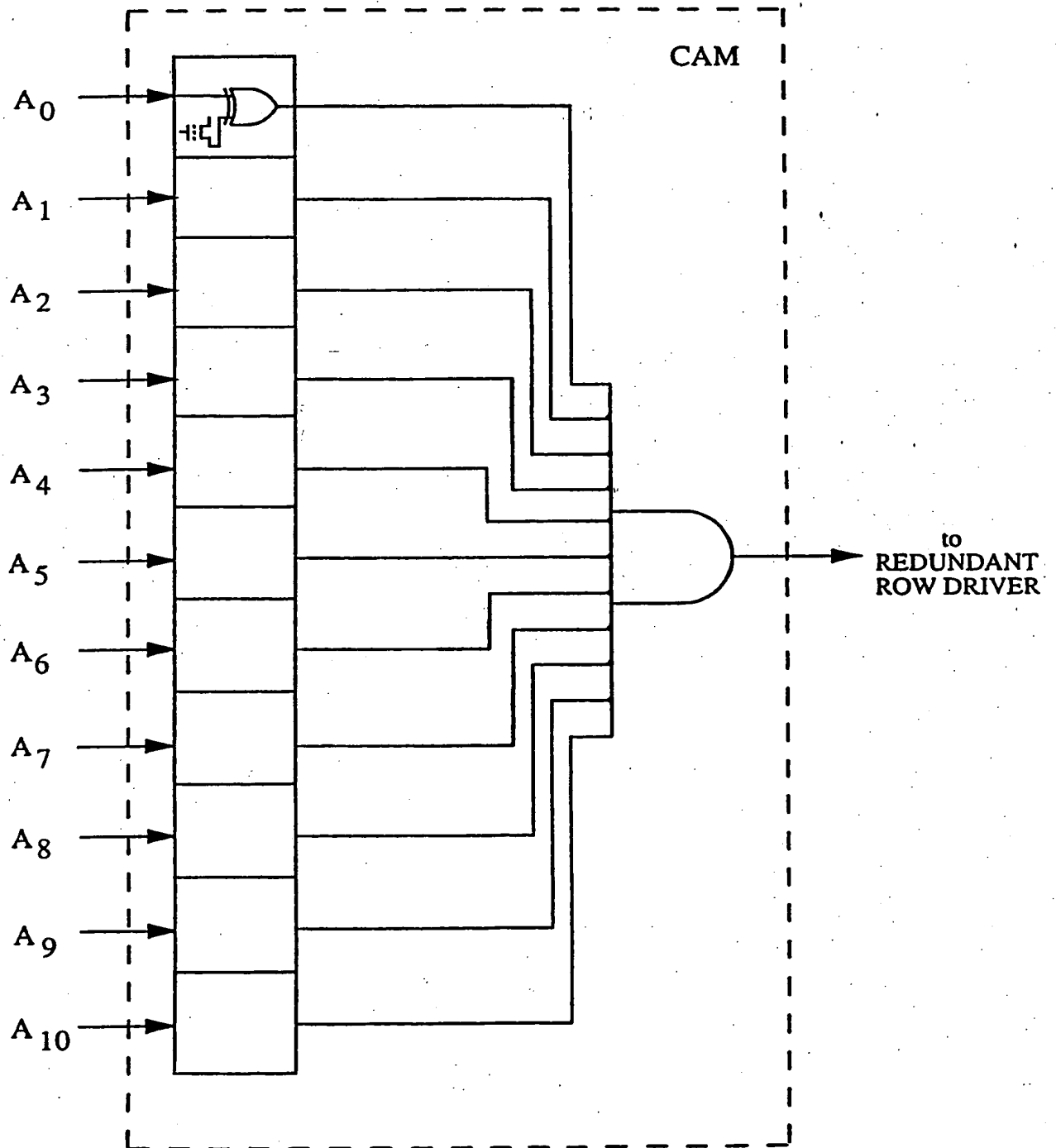


FIGURE 6



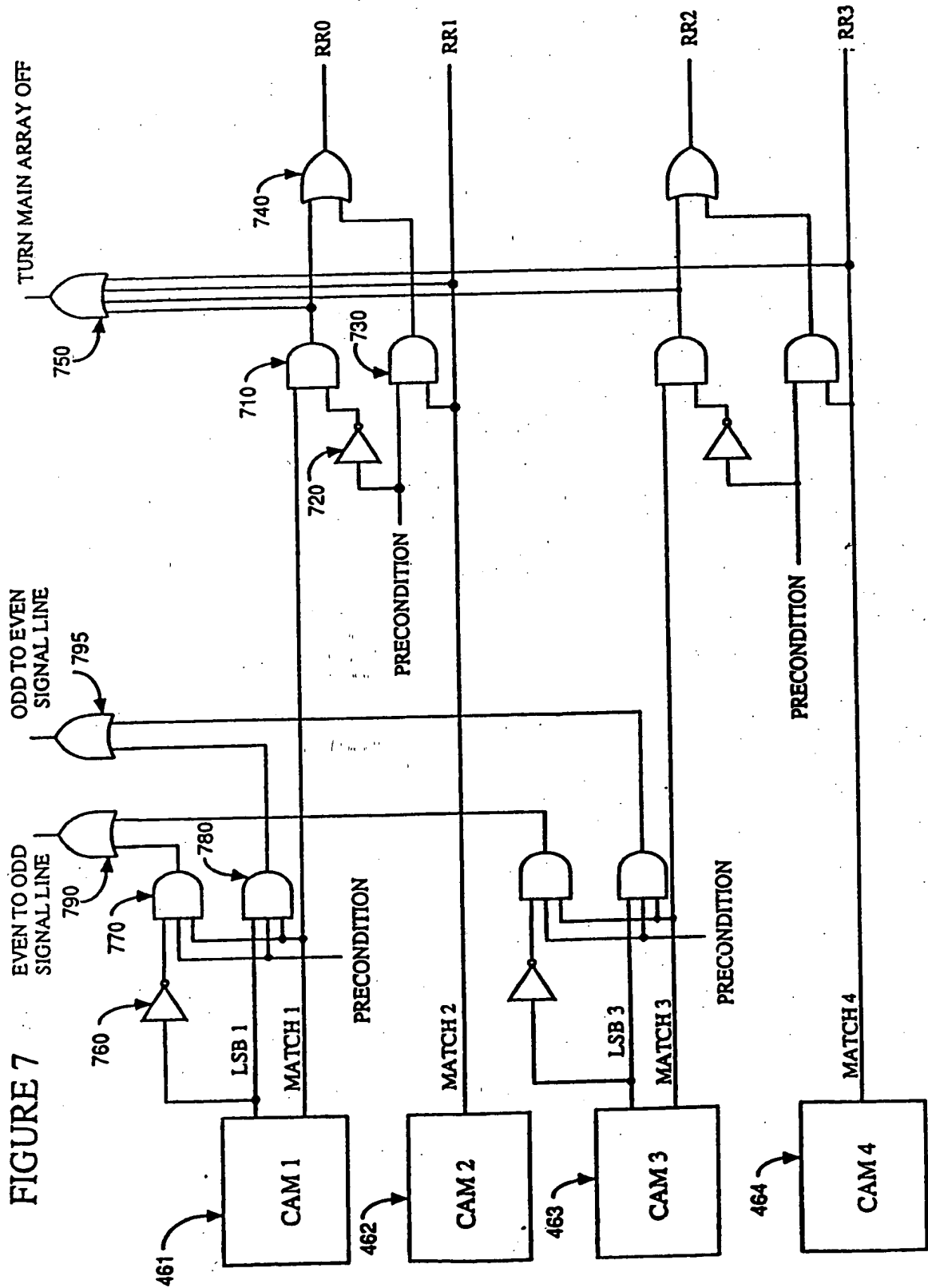


FIGURE 8 (PRIOR ART)

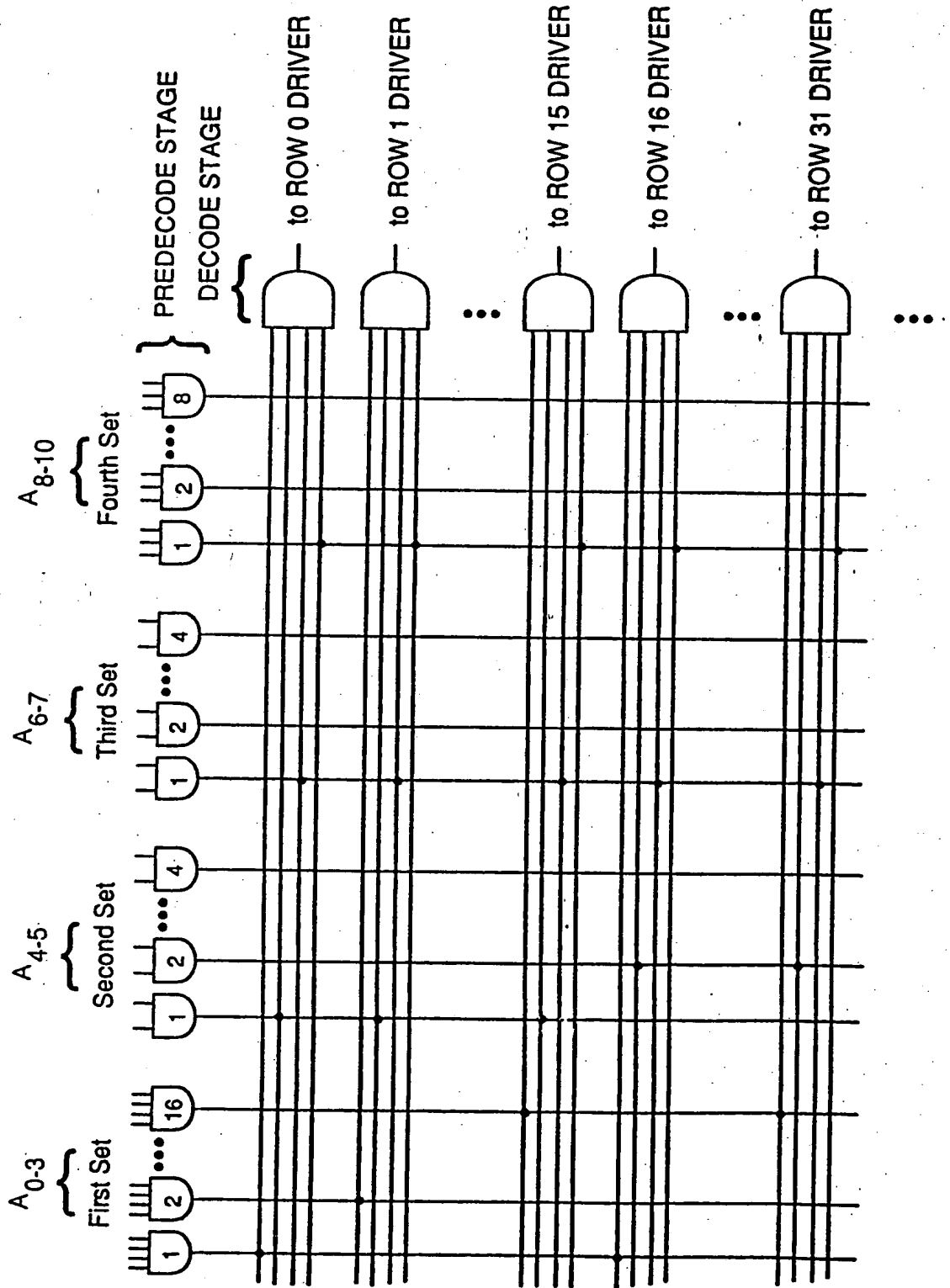
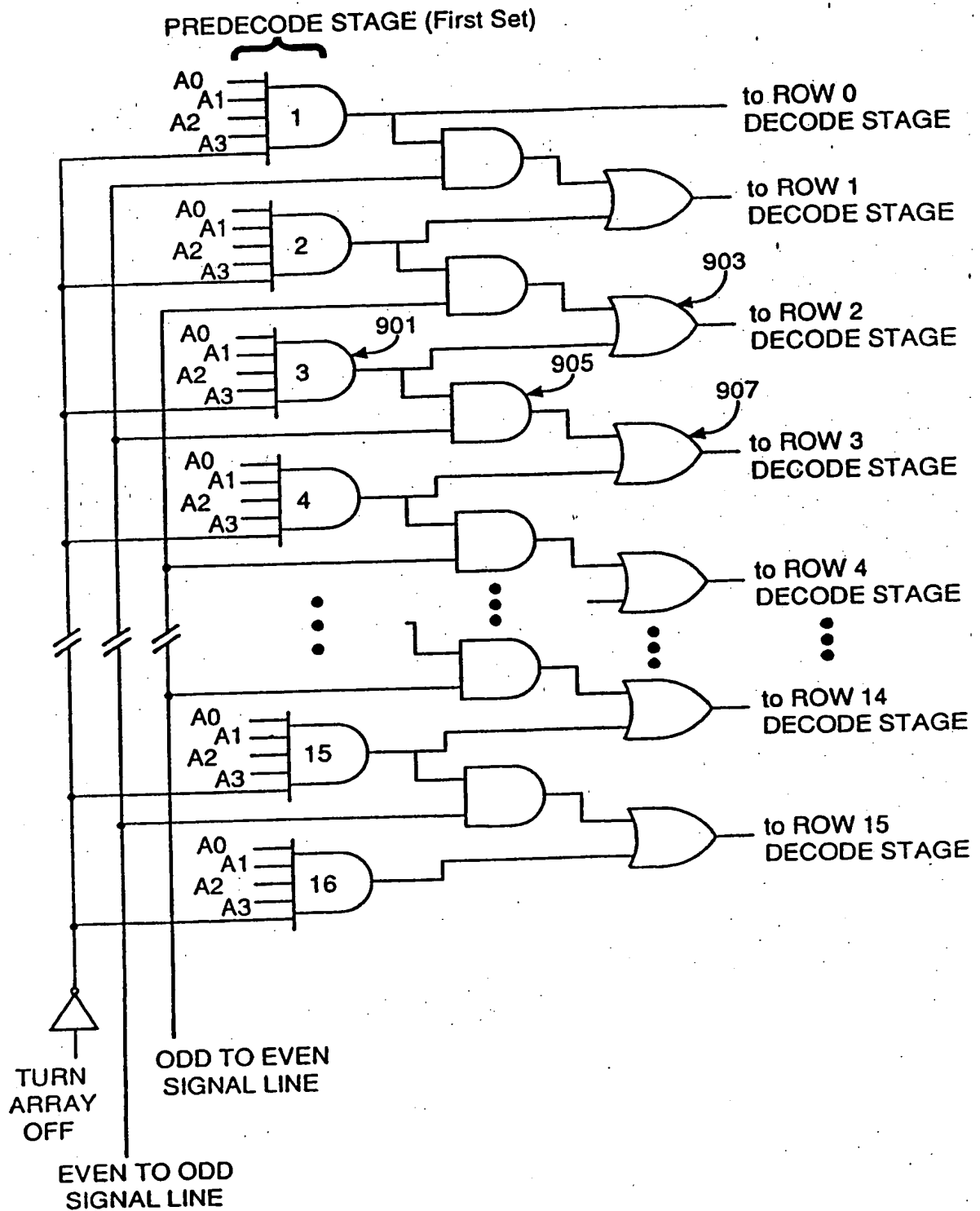


FIGURE 9



ROW REDUNDANCY FOR FLASH MEMORIES

FIELD OF THE INVENTION

The present invention relates to the field of non-volatile semiconductor memories. More specifically, the present invention relates to the field of electrically programmable read-only memories, particularly those employing floating gate memory devices.

BACKGROUND OF THE INVENTION

10 Metal-Oxide-Semiconductor (MOS) electrically programmable read-only memories (EPROMS) frequently use memory cells that have electrically isolated gates (floating gates). These floating gates are typically completely surrounded by insulation and formed from a polycrystalline silicon (polysilicon) layer. Information is stored in the memory cells or devices in the form of charge on the floating gates. Charge is transported to the floating gates by a variety of mechanisms such as avalanche injection, channel injection, tunnelling, etc., depending on the construction of the cells. The cells are erased generally by exposing the array to ultraviolet radiation. An example of these cells can be found in U.S. Patents 3,500,142; 3,660,819; 3,755,721; and 4,099,196. In some cases these cells are electrically erasable (EEPROM cells). An example of such a cell is shown in U.S. Patent 4,203,158.

The invention of the present application is used with an EPROM cell, particularly one which is electrically erasable, commonly referred to as a "flash" EPROM cell.

25 Due to the nature and design of flash EPROM cells, the entire array must be erased in order to erase any one cell in that array. Generally, this has not

been a problem in that each row (word line) is separately addressable and each column (bit line) is either separately addressable or can be addressed in groups of 8 (comprising 1 byte). Further, prior to erasing the entire array, each memory cell in that array must be preconditioned.

5 Preconditioning is the process whereby a memory cell is programmed prior to erasure to avoid over-erasing the cell which can cause leakage within that cell resulting in false data readings. This occurs when a cell in the zero state undergoes an erase operation whereby it can be driven into the depletion mode. The column sense amplifier can read this leakage current falsely as an
10 erased cell. Therefore, proper preconditioning is necessary to avoid over-erasing a single cell which can in turn cause an entire array to be defective.

 When a row (wordline) is found to be defective by the manufacturer, it is desirable to be able to assign an alternate row to take its place. Using an alternate row can thus increase the yield of working memory chips. However,
15 due to the need to precondition each memory cell in the array prior to erasing that array, it is necessary to be able to precondition each row in the array; those that are working as well as those determined to be defective in the manufacturing test stage.

 The difficulty in preconditioning both good rows and bad rows is several
20 fold. First of all, because an alternate row has been set to take the place of the bad row, it may be difficult to address or access the bad row without also accessing the alternate row. Secondly, even if one could separately address the bad row, if the defect which caused that row to be bad was due to a short between that row and a neighboring row, then merely addressing the first bad
25 row would not be sufficient to be able to precondition (program) that first bad row because it would merely short to the neighbor just as it did during

manufacturing test. Thirdly, it was previously believed to not be possible to precondition both bad rows simultaneously as it was felt that one of the two bad rows would predominate by stealing all the current thus allowing it to be preconditioned but not allowing the other bad row to be preconditioned thus still exposing the other bad row (and thus the entire array) to the over-erasure problem.

SUMMARY AND OBJECTS OF THE INVENTION

One object of the present invention is to provide a memory array with redundant rows.

Another object of the present invention is to provide a memory array with
5 redundant rows such that both defective rows and redundant rows are preconditioned.

These and other objects of the present invention are provided for by a memory array having a plurality of electrically programmable and electrically erasable memory cells each having a source region, drain region, floating gate
10 and control gate. A plurality of bit lines are used, each of which is arranged in columns and is coupled to the drain regions of the memory cells in the column. The memory array has a first word line coupled to the control gate of each cell in a first row, a second word line coupled to the control gate of each cell in a second row, a third word line coupled to the control gate of each cell in a third
15 row and a fourth word line coupled to the control gate of each cell in a fourth row. There is a means for decoding row addresses and for selecting word lines, such that if the first row is addressed for a read operation and if the first row is not functioning properly the third word line is selected, and if the second row is addressed for a read operation and if the second row is not functioning properly
20 the fourth word line is selected. There is also a means for selecting a plurality of bit lines and for coupling the source regions of the memory cells coupled to the selected bit lines to a first potential for a programming operation, for coupling the source regions of the memory cells to the first potential for a read operation, and for coupling the source regions of the memory cells to a second potential
25 for an erasure operation.

More specifically, during a preconditioning operation of the memory array, if the first row is addressed and if the first row is not functioning properly the decoding means selects the first word line and the second word line, and if the second row is addressed and if the second row is not functioning properly the decoding means selects the third word line and the fourth word line.

These and other objects are also provided for by a method of accessing alternate word lines in a memory array having a plurality of electrically programmable and electrically erasable memory cells each having a source region, drain region, floating gate and control gate. The memory array comprises a plurality of bit lines arranged in columns, each bit line coupled to the drain regions of the memory cells in the column. The memory array further comprises a first word line coupled to the control gate of each cell in a first row, a second word line coupled to the control gate of each cell in a second row, a third word line coupled to the control gate of each cell in a third row, and a fourth word line coupled to the control gate of each cell in a fourth row. The method comprises the steps of 1) if the first row is addressed for a read operation and if the first row is not functioning properly the third word line is selected, 2) if the second row is addressed for a read operation and if the second row is not functioning properly the fourth word line is selected, and 3) selecting a plurality of bit lines and coupling the source regions of the memory cells coupled to the selected bit lines to a first potential for a programming operation, to the first potential for a read operation, and to a second potential for an erasure operation.

More specifically, the method further comprises the step of 4) if the first row is addressed during a preconditioning operation and if the first row is not functioning properly the first word line and the second word line are selected,

and 5) if the second row is addressed during a preconditioning operation and if the second row is not functioning properly the third word line and the fourth word line are selected.

Other objects, features, and advantages of the present invention will be
5 apparent from the accompanying drawings and from the detailed description
which follows below.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like references indicate similar elements, and in which:

5

FIG. 1 is a cross-sectional elevation view of a prior art non-volatile floating gate memory device or cell used in the currently preferred embodiment of the present invention;

10

FIG. 2 is a block diagram of the layout of a prior art memory device;

FIG. 3 is a block diagram of the layout of a memory device of the present invention;

15

FIG. 4 is a logic diagram of a prior art X decoder used in the currently preferred embodiment of the present invention;

FIG. 5 is a logic diagram of a two stage X decoding scheme of the prior art configured to select 1 of 2048 addresses;

20

FIG. 6 depicts a content addressable memory of the prior art configured to support an 11 bit address;

25

FIG. 7 is a logic diagram showing the connections between the CAMS, the redundant row drivers, and the main array;

8

FIG. 8 is a more detailed logic diagram of the two stage X decoding scheme of Figure 5;

FIG. 9 is a logic diagram of the even/odd defective word line pairing
5 scheme of the present invention.

DETAILED DESCRIPTION

A method and apparatus for providing row redundancy in non-volatile semiconductor memories is disclosed. In the following description, numerous specific details are set forth, such as specific materials, devices, process steps, dimensions, sequences, etc., in order to provide a thorough understanding of the present invention. It will be obvious, however, to one skilled in the art that these specific details need not be employed to practice the present invention. In other instances, well-known processing steps and device configurations are not described in detail in order not to unnecessarily obscure the present invention.

Referring now to Figure 1, the memory device or cell used with the presently preferred embodiment is formed on a silicon substrate such as the p-type substrate 15 of Figure 1. Please note that the device of Figure 1 is shown in a partially fabricated state since this best reveals its structure. The device includes a pair of spaced-apart doped regions disposed in the substrate, specifically a drain region 12 and a source region 13. A polysilicon floating gate 10 is generally disposed above and between these regions and insulated from these regions by a layer of silicon dioxide or other insulative layer 14. The floating gate 10, at the completion of the processing, is completely surrounded by insulative layers and, hence, electrically floats. A second gate (control gate 11) is disposed above the floating gate 10; in the presently preferred embodiment this gate is fabricated from a second layer of polysilicon. This control gate is a continuous polysilicon strip forming a word line of the memory array of Figure 2.

It will be appreciated that the cell of Figure 1 may be fabricated using well-known NMOS or CMOS technology. The n-channel device illustrated in

Figure 1 may be fabricated directly in a p-type substrate or, when an n-type substrate is used, may be fabricated in a p-type well formed in the substrate. Other variations, such as employing both p-wells and n-wells, are well known in the art.

5 As currently employed, the memory devices are programmed (i.e., negatively charging the floating gate) by coupling the word line or control gate 11 to a potential of approximately +12 volts, the drain region to a potential of approximately +7 volts, and the source region to ground. With these conditions, channel hot electron injection occurs through the oxide layer 14 which layer, in
10 the currently preferred embodiment, is approximately 115 Å thick.

 To erase the cell, the drain region is floated, the word line or control gate 11 is grounded, and a potential of approximately +12 volts is applied to the source region. Under these conditions charge is tunneled from the floating gate.

15 During reading of the cell, a positive potential less than that which would cause charge to transfer onto the floating gate is applied to the control gate (e.g., 5 volts) and a potential (e.g., 1 volt) is applied to the drain region. Current through the device is sensed to determine if the floating gate is or is not negatively charged. As with other floating gate devices, the negative charge on
20 the floating gate shifts the threshold voltage of the device making it less conductive. Thus, with a sense amplifier, the presence or absence of charge on the floating gate can be determined. This defines whether a cell is programmed with a binary one or zero.

 Referring now to Figure 2, the memory cells of a flash memory array are
25 formed at intersections of word lines and bit lines, as is the common practice. The drain terminals of the memory cells are coupled to the bit lines. The control

gates are formed from continuous strips of polysilicon which extend across the entire array to form the word lines. The generally parallel bit lines are perpendicular to the generally parallel word lines. For example, in memory array 40, cell 27 has its drain region coupled to bit line 38 and its source region 39 coupled to source switch 50. The word line 29 extends to a plurality of other cells along the word line. The source regions for all the cells in memory array 40 are connected to a common node allowing this node to be switched to different potentials by source switch 50.

The X decoder 43 selects a single word line in memory array 40 for each of the addresses AX_0 - AX_m applied to it. The Y decoders select one byte (8 bit lines) from memory array 40 for each of the Y addresses AY_0 - AY_n and couples 8 bit lines from memory array 40 to the sense amplifier and output buffers 54. Source switch 50 is controlled by Y decoder 44 and causes the source regions of the cells in the memory array to be coupled to the different potentials for reading, programming, and erasing.

Referring now to Figure 3, the memory array and control means of the present invention can be seen. The memory array of the present invention is comprised of main array 40 and redundant rows 48. X decoder 43 decodes addresses AX_0 - AX_m to select one word line of main array 40. The decoded address from X decoder 43 is input to one word line driver of drivers 45 to thus drive the selected word line (e.g., word line 29) of main array 40. Y decoder 44 decodes addresses AY_0 - AY_n to select one byte (8 bit lines) from main array 40 and redundant rows 48. Please note that source Y decoder 60, source switch 50 and sense amplifiers and output buffers 54 of Figure 2 are not shown in Figure 3 to aid in clarity.

Referring now to Figure 4, a simplified logic diagram of X decoder 43 can be seen. X decoder 43, comprised of multiple decoders (only the first 8 decoders are shown in Figure 4) which decode addresses $AX_0 - AX_m$ to select a single driver to drive one of the word lines of the memory array, can be most easily understood as a series of multiple input AND logic gates.

An AND logic gate, as is well known in the art, will provide a high output signal when all of its input signals are high. However, through the proper selection of inverters (not shown in Figure 4), an AND gate can provide a high output signal for any combination of possible inputs. For example, if a particular AND gate is to be used to select the word line associated with the address of zero (all input signals low), then each of the inputs would merely need to first pass through an inverter to raise all of the input signals high. Similarly, for the address of one (all high order input signals low while the least significant bit input signal is high), then each of the high order inputs would first pass through an inverter while the least significant bit input signal would pass directly to the AND gate in order to achieve an all input signal high condition. Continuing in this fashion, all of the possible combinations of address input signals can be decoded by merely placing different combinations of inverters on the inputs to the AND gates.

In the preferred embodiment of the present invention there are 2048 word lines. As such, the decoders of X decoder 43 decode 1 of 2048 possible word line addresses. Therefore, each of the decoders of X decoder 43 of Figure 4 can be represented by an 11-input (addresses $A_0 - A_{10}$) AND gate which, again through proper selection of front-end inverters, can select 1 of 2048 combinations. Again, please note that only the first 8 of the total 2048 11-input AND gate decoders of X Decoder 43 are shown in Figure 4.

Although AND gates with numerous inputs most easily explain how the decoders of X Decoder 43 can select 1 of 2048 (or any other number of potential combinations one may need to select from), using numerous-input AND gates is not practical due to chip size and power requirements. Instead, a cascade of AND gates is used as can be seen with reference to Figure 5.

Figure 5 shows a two stage X decoding scheme, as is used in the preferred embodiment of the present invention, configured to select 1 of 2048 word lines. The first stage, or predecode stage, takes groups of the address input signals $AX_0 - AX_m$ and inputs them to a parallel set of AND gates. The second stage, or decode stage, takes the output of the first stage and selects one of the 2048 word line drivers of Drivers 45 which in turn drives one of the word lines of Main Array 40.

The predecode stage is made up of 4 sets of AND gates. The first set is comprised of 16 4-input AND gates each of which receives as input the four low order (least significant) address bits (denoted A_0-A_3 in Figure 5 and which correspond to AX_0-AX_3 of Figures 2 & 3). Each of the 16 4-input AND gates of the first set outputs a different predecode signal, again due to different combination of inverters placed on their input signal lines. In this way, the 16 4-input AND gates of the first set of the predecode stage can decode all 16 possible combinations from the low order 4 bits of the input address.

The second set of the predecode stage is comprised of 4 2-input AND gates each of which receives as input the next 2 significant address bits (denoted A_4-A_5 in Figure 5 and which correspond to AX_4-AX_5 of Figures 2 & 3). Each of the 4 2-input AND gates of the second set outputs a different predecode signal, again due to different combinations of inverters placed on their input signal lines. In this way, the 4 2-input AND gates of the second set of the

predecode stage can decode all 4 possible combinations from the next 2 significant bits of the input address.

The third set of the predecode stage is also comprised of 4 2-input AND gates each of which receives as input the next 2 significant address bits (denoted A₆-A₇ in Figure 5 and which correspond to A_{X6}-A_{X7} of Figures 2 & 3). Each of the 4 2-input AND gates of the third set outputs a different predecode signal, again due to different combinations of inverters placed on their input signal lines. In this way, the 4 2-input AND gates of the third set of the predecode stage can decode all 4 possible combinations from the next 2 significant bits of the input address.

The fourth set of the predecode stage is comprised of 8 3-input AND gates each of which receives as input the 3 most significant address bits (denoted A₈-A₁₀ in Figure 5 and which correspond to A_{X8}-A_{X_m} of Figures 2 & 3). Each of the 8 3-input AND gates of the fourth set outputs a different predecode signal, again due to different combinations of inverters placed on their input signal lines. In this way, the 8 3-input AND gates of the fourth set of the predecode stage can decode all 8 possible combinations from the 3 most significant bits of the input address.

The decode stage of X decoder 43 is made up of 2048 4-input AND gates each of which receives as input a different combination of 4 outputs from the predecode stage to thus decode the 2048 possible address combinations. Each of the 2048 4-input AND gates of the decode stage in turn selects a different row driver to thus drive the selected word line in Main Array 40.

With reference to Figure 8 a more detailed view of the two stage decoding scheme of Figure 5 can be seen. In Figure 8, the predecoding stage (comprising 4 sets of AND gates) is shown having vertical outputs which

intersect at different points the horizontal inputs of the decoding stage (comprising 2048 4-input AND gates). These intersections of predecoding stage outputs and decoding stage inputs more clearly show the varying inputs to the decoding stage from the predecoding stage.

5 As can be seen in Figure 8, the inputs to the 4-input AND gate of the decode stage which signals the row 0 driver receive as a first input signal the output from the first 4-input AND gate of the first set of the predecode stage. Conversely, the inputs to the 4-input AND gate of the decode stage which signals the row 1 driver receive as a first input signal the output from the second
10 4-input AND gate of the first set of the predecode stage.

Similarly, the inputs to the 4-input AND gate of the decode stage which signals the row 15 driver receive as a first input signal the output from the sixteenth 4-input AND gate of the first set of the predecode stage. However, the inputs to the 4-input AND gate of the decode stage which signals the row 16
15 driver receive as a first input signal the output from the first 4-input AND gate of the first set of the predecode stage just as the 4-input AND gate which signals the row 0 driver did. However, in order to decode addresses which vary by more than 16, the inputs to the 4-input AND gate of the decode stage which signals the row 16 driver receive as a second input signal the output from the
20 first 2-input AND gate of the second set of the predecode stage.

The inputs to the remaining AND gates of the decode stage of X decoder 43 continue in this progressive selection of varying combinations of output signals from the predecode stage. In this way, and as stated above, the 4-input AND gates of the decode stage (together with the 4 sets of AND gates of the
25 predecode stage) of X decoder 43 can decode each of the different input addresses and can signal a different row driver in each case.

Referring again to Figure 3, if a defective word line is discovered (e.g., one word line is found to be shorted to another word line) when main array 40 is tested following production of the device, an alternate word line in redundant rows 48 may be selected by the manufacturer by setting the address of the shorted word line in one of the Content Addressable Memories (CAMS) of CAMS 46 (CAM operation is discussed in more detail below). In this way, when a defective word line in main array 40 is later addressed by the user, the CAM in CAMS 46 which is set to that address will select the associated driver in drivers 47 to drive the alternate word line in redundant rows 48 instead of the defective word line in main array 40.

Referring now to Figure 6, one CAM of CAMS 46 can be seen. A CAM can be most easily understood as a set of comparison blocks (one for each bit of the input address) whose outputs are fed into a single multiple-input AND gate. Each comparison block contains both a memory cell set to one address bit and an Exclusive NOR (XNOR) gate to do the comparison. Each address $AX_0 - AX_m$ ($A_0 - A_{10}$ in the preferred embodiment) is input to each CAM where each comparison block checks its relevant bit.

In other words, when a word line of main array 40 is addressed each CAM of CAMS 46 individually checks for a match with one of the alternate redundant row word lines. Each bit of the input address is checked within each CAM by comparing the stored bit in the memory cell with one bit of the input address. The comparison is done with an XNOR gate which will only output a high signal when both of its inputs are the same, either both high or both low, as is well known in the art.

The AND gate of the CAM receives as inputs the output of each of the XNOR gates in the comparison blocks. The AND gate will only output a high

signal if each comparison block is outputting a high signal. That is, the AND gate will only drive the word line driver for its associated redundant row if every comparison block in that CAM finds a match between its stored address bit and the incoming address bit. In this way, when the address of the defective word line in main array 40 is set in one of the CAMS of CAMS 46, when that address is input to the memory array the alternate word line in redundant rows 48 is selected by that CAM.

Of course, merely selecting and driving an alternate word line does not by itself avoid using the defective word line in main array 40. This is because the decoder in X decoder 43 will still decode that address and will thus drive the defective word line. Then, because the 8 bit lines selected by Y decoder 44 connect to all the drains of the memory cells of both main array 40 and redundant rows 48, merely driving an alternate word line in Redundant Rows 48 will not by itself prevent attempting to read or write to the defective word line in main array 40. Additional logic circuitry is therefore used to turn main array 40 off as needed.

However, when main array 40 (along with redundant row 48) is erased, because the entire main array 40 and all of the word lines of redundant row 48 will be erased (again, due to the nature of flash memory), each row must first be preconditioned. Preconditioning is programming prior to erasure to avoid over erasing the memory cells which could cause them to go into depletion which then causes the entire array to fail.

Referring now to Figure 7, when CAM 1 (reference number 461) finds a match between the input address $AX_0 - AX_m$ and the set of stored address bits, CAM 1 will output a high signal on MATCH 1 signal line. This high signal is intended to drive the word line driver for the alternate redundant row when the

address is being used for a read or write operation. During a read or write operation (as opposed to a precondition operation) the input to inverter 720 is a low signal in which case the output of inverter 720 is a high signal. Thus during a read or write operation AND gate 710 sees high signals on both of its inputs
 5 and will therefore output a high signal. OR gate 740, receiving the high output signal from AND gate 710 will thus output a high signal on RR0 which is the signal line to the driver of drivers 47 which will in turn drive the alternate word line in redundant rows 48.

Note that the output of AND gate 710 is also input to OR gate 750. OR
 10 gate 750, seeing a high input signal from AND gate 710 during a read or write operation, will output a high signal to turn main array 40 off. The connection and function of the output signal line from OR gate 750 to main array 40 will be discussed more fully below.

Thus, during a read or write operation, when CAM 1 decodes a match
 15 between its stored address and its input address it will not only signal its associated driver to drive the alternate word line in redundant rows 48 but it will also signal main array 40 to turn off. In this way, the desired alternate good row will be selected instead of the defective bad row.

Further, as can be seen by the four inputs to OR gate 750, whenever any
 20 one of the four CAMS numbered 461-464 as shown in Figure 7 detects a match between its stored address and an input address, during either a read or a write operation, OR gate 750 will signal main array 40 to turn off.

If an erase operation is to be performed a precondition operation should first be done for the reasons discussed above. When a precondition operation
 25 is to be performed inverter 720 receives a high input signal and thus provides a low output signal. Then, although CAM 1 (reference number 461) may be

outputting a high MATCH 1 signal, AND gate 710 outputs a low signal due to the low input signal from inverter 720. Therefore, although a match may be found by CAM 1, OR gate 740 will not provide a high output signal to the driver for redundant row 0 (RR0) because neither of its input signals is high.

5 Additionally, although a match may have been found by CAM 1, due to the low output signal from AND gate 710 OR gate 750 will not output a high signal to turn main array 40 off. In other words, although a match is found by CAM 1, neither the redundant row is selected nor is main array 40 turned off during a precondition operation on the address set in CAM 1.

10 Of course, the objective during a precondition operation is to precondition both the defective row (and its defective neighbor) as well as the alternate redundant rows. This is because, as stated above, if any individual row is not preconditioned before the entire memory array is erased, the entire memory array is eventually exposed to leakage from over-erasure of the one or
15 more cells along that word line which was not preconditioned prior to erasure. Preconditioning all of the word lines, both good ones and bad ones, is thus necessary.

As stated above, CAM 1 (reference number 461) outputs a high signal when a match is found between the input address and the address stored in
20 CAM 1. Then prior to an erasure operation, AND gates 770 and 780 help determine which rows in Main Array 40 get selected for preconditioning. In other words, when CAM 1 outputs a high signal and when a precondition operation is occurring, either AND gate 770 or AND gate 780 will output a high signal depending upon whether the least significant bit of the input address to
25 CAM 1 is high or low.

In other words, if the least significant bit of the input address to CAM 1 is low (in which case the input address is an even address) then inverter 760 will provide a high input signal to AND gate 770 which will in turn provide a high input signal to OR gate 790. Conversely, if the least significant bit of the input address to CAM 1 is high (in which case the input address is an odd address) then CAM 1 will provide a high input signal to AND gate 780 who will in turn provide a high input signal to OR gate 795.

In this way, during a precondition operation whenever there is a match between an input address to CAM 1 and the address stored in CAM 1, either OR gate 790 will provide a high output signal (thus indicating that the input address was even) or OR gate 795 will provide a high output signal (thus indicating that the input address was odd).

Remembering that the objective is to precondition each row (defective as well as functioning) of the memory array before erasing the entire memory, the even/odd address signal lines are used to indicate which additional word line in main array 40 will be selected when a CAM finds a match during a precondition operation. And because inverter 720, by outputting a high signal during a precondition operation, prevented AND gate 710 from outputting a high signal to both OR gate 750 and OR gate 740, neither redundant row RR0 is selected nor is main array 40 turned off. Therefore, during a precondition operation when a defective row in main array 40 is addressed the word line in main array 40 is selected and main array 40 will not be turned off. Further, its neighboring defective word line will also be selected, as is explained below, through the use of the even/odd signal lines from OR gates 790 and 795.

Selecting both the addressed word line and the neighboring word line in main array 40 enables a precondition operation of a defective word line and its

neighbor. Because an electrical short between adjacent row word lines is a prevalent form of row defects, it has been discovered that one way to precondition a shorted word line is to select both word lines which are shorted together to thus precondition them together.

5 Referring now to Figure 9, a portion of the predecode stage (the first set of Figure 5) of X decoder 43 of main array 40 can be seen. The array off signal from OR gate 750 of Figure 7 can be seen in the lower left hand corner of Figure 9. Additionally, both the even to odd signal line from OR gate 790 of Figure 7 and the odd to even signal line from OR gate 795 of Figure 7 can be seen in the
10 lower left hand corner of Figure 9.

Figure 9 shows the first set of 16 4-input AND gates of the predecode stage of X decoder 43 of main array 40. Figure 9, however, includes 5-input AND gates instead of the 4-input AND gates wherein the fifth input is the inverted Array Off signal from OR gate 750 of Figure 7. In this way, when OR
15 gate 750 of Figure 7 is high (indicating a match between one of the CAMS in CAMS 46 during a read or write operation), none of the 16 5-input AND gates of the first set of the predecode stage of X Decoder 43 shown in Figure 9 will output a high signal and therefore none of the 2048 4-input AND gates of the decode stage of X decoder 43 will output a high signal and therefore none of
20 the drivers in drivers 45 will drive any of the word lines in main array 40.

Conversely, when a CAM in CAMS 46 find a match during a precondition operation, OR gate 750 will output a low signal which, when inverted prior to being inputted to the 16 5-input AND gates, will cause the entire main array 40 to be operational (because each of the 16 5-input AND gates will see a high
25 signal thus effectively turning the array on). Further, during a precondition operation when a CAM finds a match, either the even to odd signal line will

necessarily be high or the odd to even signal line will necessarily be high.

Then, because main array 40 is operational, the one decoder of X decoder 43 which has decoded the input address and selected its associated driver will cause the selected word line in main array 40 to be driven.

- 5 If the driven word line in main array 40 is an even address word line, for example if the selected word line address corresponds to row 2, then the output of the 5-input AND gate 3 (reference number 901) will be a high signal to OR gate 903 which will in turn signal the decode stage of X Decoder 43 to select row 2 of Main Array 40. Additionally, because row 2 is an even address, the
- 10 even to odd signal line will have been driven high (as explained above) by OR gate 790 of Figure 7. Because the high output from AND gate 901 is also input to AND gate 905, when the even to odd signal line (also input to AND gate 905) also goes high, AND gate 905 will output a high signal. When AND gate 905
- 15 outputs a high signal OR gate 907 will output a high signal to the decode stage of X decoder 43 which will cause the driver of row 3 in drivers 45 to drive the word line for row 3. Note that if the input address had been an odd address then the odd to even signal line would have been high and the neighbor row to the odd addressed word line in main array 40 would have selected.

- 20 In this way, whenever a precondition operation is performed and a match is found by a CAM, both the input address row word line and the adjacent odd/even address row word line of main array 40 are selected. This enables addressing both shorted word lines in main array 40 so as to be able to precondition them prior to erasure of the entire memory array.

- 25 As for preconditioning the redundant rows, because the precondition signal caused the first redundant row RRO of redundant rows 48 to not be selected (as explained above), something else must occur in order to

precondition that word line. Additionally, the neighboring redundant word line (which is the alternate row word line for the second of the pair of shorted word lines in main array 40) must also be preconditioned prior to erasing the entire memory array. Addressing the two redundant rows RR0 and RR1 in redundant rows 48 is achieved as follows with reference again to Figure 7.

In Figure 7, when the preconditioning operation reaches the second address of the pair of redundant rows, CAM 2 (reference number 462) sees a match between its stored address and the input address. CAM 2 therefore outputs a high signal to the driver in drivers 47 to drive the second alternate word line in redundant rows 48. When CAM 2 outputs a high signal on RR2, OR gate 750 sees this high input and signals main array 40 to turn off.

The high output signal from CAM 2 is also input to AND gate 730 which, together with the high precondition signal, causes AND gate 730 to output a high signal to OR gate 740. OR gate 740, upon seeing the high input signal from AND gate 730 will signal the driver in drivers 47 to drive the first alternate word line in redundant rows 48.

Therefore, when CAM 2 finds a match during a precondition operation, both the first and the second alternate word lines are selected in redundant rows 48 while main array 40 is turned off. In this way, when the second of a pair of shorted word lines is addressed during a precondition operation, both of the two redundant word lines in redundant rows 48 is selected and the main array 40 is turned off. Please note that CAM 3 and CAM 4 operate essentially identically to CAM 1 and CAM 2 as they are merely supporting a second set of redundant row word lines. Multiple pairs of redundant rows can be supported by this scheme while only two sets of two redundant rows have been shown.

The logic, as shown in Figure 9, which selects shorted row word line pairs within main array 40 during a precondition operation and which is placed between the predecode stage and the decode stage of X decoder 43, can select either row 0 and row 1, or row 1 and row 2, or row 2 and row 3, etc. This pair selection, as was explained above, depends upon which rows were determined to be shorted together, X decoder 43 selecting the first row word line of the pair, and whether a precondition operation is being performed, among other things. However, in the preferred embodiment of the present invention, if row 15 and row 16 are shorted together and there is an attempt to select row 15 and row 16 during a precondition operation row 16 would not be selected.

To understand why both row 15 and row 16 would not be selected during a precondition operation one must first remember that the X decoder 43 is optimized (based on chip space and power requirements) to decode 1 of 2048 word line addresses by grouping the input address bits into four sets of AND gates (as was discussed with reference to Figures 5 and 8). Then, because the logic which selects the next even (or odd, as appropriate) row word line of main array 40 is located between the first set of 16 AND gates of the predecode stage and the 2048 AND gates of the decode stage of X decoder 43 the resolution of this logic to pairs within each multiple of 16 row word lines of main array 40 is thus limited. In other words, because the first set of AND gates of the predecode stage is shared by each multiple of 16 row addresses (again, to optimize X decoder 43), placing the pair selection logic only on the output of this set of the predecode stage necessarily limits the pair selection to pairs within each group of 16 row word lines.

This limitation, overcome in alternative embodiments as explained below, can be more easily explained with reference again to Figure 8. The X decoding scheme of the preferred embodiment as can be seen in Figure 8 shows that the first AND gate of the first set of the predecode stage of X decoder 43 is shared by the AND gates of row 0 and row 16 (and row 32, 48, 64, etc.) of the decode stage of X decoder 43.

In further explanation, the only difference in inputs to the AND gates of row 0 and row 16 is the connection from the second set of AND gates of the predecode stage. That is, to decode 1 of 2048 address the AND gate of row 0 receives as its 4-inputs the output of i) the first AND gate of the first set of the predecode stage; ii) the *first* AND gate of the second set of the predecode stage; iii) the first AND gate of the third set of the predecode stage; and, iv) the first AND gate of the fourth set of the predecode stage. Similarly, to decode 1 of 2048 addresses the AND gate of row 16 receives as its 4-inputs the output of i) the first AND gate of the first set of the predecode stage; ii) the *second* AND gate of the second set of the predecode stage; iii) the first AND gate of the third set of the predecode stage; and, iv) the first AND gate of the fourth set of the predecode stage.

Therefore, when the logic which selects shorted row word line pairs is placed only on the first set of AND gates of the predecode stage (as in the preferred embodiment of the present invention), this logic is unable to select the row word line pair of row 15 and its next even neighbor (row 16) because there is no AND gate (such as AND gate 905 of Figure 9) to signal an OR gate (such as OR gate 907 of Figure 9) to signal the driver for row 16. Note that essentially the same situation occurs between rows 31 and 32, rows 47 and 48, etc.

Of course, it is possible to add the logic which selects shorted row word line pairs to the outputs of each set of AND gates of the predecode stage. And there is no concern about improperly selecting more than one row word line pair at a time because the logic which selects shorted row word line pairs also depends upon decoding the first row word line of the pair and therefore the only pair which would actually be selected would be the proper first row word line and its next even or odd row word line which is thus the desired shorted row word line pair.

To repeat, if the additional logic which selects the second of the shorted row word line pairs (regardless of whether that happens to be an even or an odd word line), as shown connected to the first set of AND gates of the predecode stage in Figure 9, were to be added throughout the four sets of AND gates in the predecode stage then any address combination of shorted row word line pairs could be selected during a precondition operation by X decoder 43 decoding and selecting the first shorted row word line of the pair and by the additional logic selecting the neighboring even (or odd, as the particular case may be) row word line.

The preferred embodiment of the present invention, while not able to select every sixteenth pair of shorted word lines, thus exposes each device to a 1 in 16 chance of a defect attributable to a shorted row word line which cannot be addressed by the preferred embodiment of this redundant row scheme. Alternative embodiments eliminate this exposure but require additional logic to do so. This additional logic takes up additional space on the chip thus potentially increasing die size. Therefore, in the preferred embodiment of the present invention, a balance has been struck whereby chip space

considerations outweigh the potential 6% chance of a short which might occur between every 16th row word line pair during manufacturing of the device.

Additionally, in the preferred embodiment of the present invention, during fabrication of the memory cell as discussed above with reference to Figure 1, a metal 1 layer is laid down to form the bit lines of the memory device. After laying
5 down an insulative layer a metal 2 layer is then laid down as an independent interconnect layer. The metal 2 layer forms lines paralleling the word lines of the memory device.

The metal 2 layer can be strapped (electrically connected at various
10 points or intervals across the memory array) to the underlying parallel word lines. Strapping a metal 2 line to an underlying parallel word line lowers the resistance of the word line by acting as a parallel resistor. This reduction in word line resistance allows the voltage applied to a word line to ramp much more quickly which results in improved device performance. For example,
15 through simulations and test devices with metal 2 lines strapped to the underlying word lines, roughly a 20% improvement in device read times (from approximately 100 nS to approximately 80 nS) has been shown.

In the past, strapping the metal 2 lines to the parallel word lines has been a problem because it increases the likelihood of electrical shorts between
20 neighboring word lines. Because the metal 2 lines are formed later in the fabrication process, they are formed when the device is less planar than when the earlier layers were formed. As such, the metal 2 lines must cross the hills and valleys caused during the typical chip fabrication. Crossing these hills and valleys is more difficult in that the resolution of the typical photolithography
25 process is lessened by this more irregular surface. Therefore, each metal 2 line is more likely to incur either physical separation as it attempts to traverse the

device or alternatively, to make electrical contact with a neighboring metal 2 line.

5 This exposure to electrical shorts between neighboring metal 2 lines makes strapping them to underlying word lines a risky proposition when there is no row redundancy built into the device. Stated differently, strapping metal 2 lines to underlying word lines increases device performance while also increasing the likelihood of device defects. In the past, the gains in performance have not been deemed worth this reduced device yield.

10 By providing row redundancy, metal 2 lines can now be strapped to the word lines and if a metal 2 line and word line is found to be shorted to a neighboring metal 2 line and word line then a pair of redundant rows may be assigned to take the place of the shorted rows. In this way, the improved performance gained by strapping metal 2 lines to word lines may be enjoyed without significantly affecting device yield.

15 In the foregoing specification, the invention has been described with reference to the presently preferred embodiment thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specifications and drawings are, accordingly, to be
20 regarded in an illustrative rather than a restrictive sense.

CLAIMS

1. A memory array having a plurality of electrically programmable
5 and electrically erasable memory cells each having a source region, drain
region, floating gate and control gate, the memory array comprising:
a plurality of bit lines arranged in columns, each bit line coupled to the
drain regions of the memory cells in the column;
a first word line in a first row, the first word line coupled to the control gate
10 of each cell in the first row;
a second word line in a second row, the second word line coupled to the
control gate of each cell in the second row;
a third word line in a third row, the third word line coupled to the control
gate of each cell in the third row;
15 a fourth word line in a fourth row, the fourth word line coupled to the
control gate of each cell in the fourth row;
means for decoding row addresses and for selecting word lines, such
that if the first row is addressed for a read operation and if the first row is not
functioning properly the third word line is selected, and if the second row is
20 addressed for a read operation and if the second row is not functioning properly
the fourth word line is selected;
means for selecting a plurality of bit lines and for coupling the source
regions of the memory cells coupled to the selected bit lines to a first potential
for a programming operation, for coupling the source regions of the memory
25 cells to the first potential for a read operation, and for coupling the source
regions of the memory cells to a second potential for an erasure operation.

2. In the memory array of Claim 1, wherein during a preconditioning operation, if the first row is addressed and if the first row is not functioning properly the decoding means selects the first word line and the second word
5 line.

3. In the memory array of Claim 1, wherein during a preconditioning operation if the second row is addressed and if the second row is not functioning properly the decoding means selects the third word line and the
10 fourth line.

4. The memory defined by Claim 1 wherein the first potential is ground potential.

15 5. The memory defined by Claim 1 wherein the second potential is approximately +12 volts.

6. A memory array having a plurality of electrically programmable and electrically erasable memory cells each having a source region, drain
20 region, floating gate and control gate, the memory array comprising:
a plurality of bit lines arranged in columns, each bit line coupled to the drain regions of the memory cells in the column;
a first word line in a first row, the first word line coupled to the control gate of each cell in the first row;
25 a second word line in a second row, the second word line coupled to the control gate of each cell in the second row;

means for decoding row addresses and for selecting word lines, such that if the first row is addressed and if the first row is not functioning properly the second word line is selected;

means for selecting a plurality of bit lines and for coupling the source regions of the memory cells coupled to the selected bit lines to a first potential for a programming operation, for coupling the source regions of the memory cells to the first potential for a read operation, and for coupling the source regions of the memory cells to a second potential for an erasure operation.

10 7. The memory defined by Claim 6 wherein the first potential is ground potential.

8. The memory defined by Claim 6 wherein the second potential is approximately +12 volts.

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9. A method of accessing alternate word lines in a memory array having a plurality of electrically programmable and electrically erasable memory cells each having a source region, drain region, floating gate and control gate, the memory array comprising a plurality of bit lines arranged in columns, each bit line coupled to the drain regions of the memory cells in the column, the memory array further comprising a first word line coupled to the control gate of each cell in a first row, a second word line coupled to the control gate of each cell in a second row, a third word line coupled to the control gate of each cell in a third row, and a fourth word line coupled to the control gate of each cell in a fourth row, said method comprising the steps of:

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if the first row is addressed for a read operation and if the first row is not functioning properly the third word line is selected, and if the second row is addressed for a read operation and if the second row is not functioning properly the fourth word line is selected;

- 5 selecting a plurality of bit lines and coupling the source regions of the memory cells coupled to the selected bit lines to a first potential for a programming operation, to the first potential for a read operation, and to a second potential for an erasure operation.

- 10 10. The method of Claim 9 wherein the first potential is ground potential.

- 15 11. The method of Claim 9 wherein the second potential is approximately +12 volts.

12. The method of Claim 9 further comprising the step of:
if the first row is addressed during a preconditioning operation and if the first row is not functioning properly the first word line and the second word line are selected.

- 20 13. The method of Claim 9 further comprising the step of:
if the second row is addressed during a preconditioning operation and if the second row is not functioning properly the third word line and the fourth word line are selected.

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14. A method of preconditioning word lines in a memory array having a plurality of electrically programmable and electrically erasable memory cells each having a source region, drain region, floating gate and control gate, the memory array comprising a plurality of bit lines arranged in columns, each bit line coupled to the drain regions of the memory cells in the column, the memory array further comprising a first word line coupled to the control gate of each cell in a first row and a second word line coupled to the control gate of each cell in a second row, the preconditioning method comprising the steps of;
- 5 if the first row is addressed and if the first row is not functioning properly, the first word line and the second word line are selected;
- 10 selecting a plurality of bit lines and coupling the source regions of the memory cells coupled to the selected bit lines to a first potential.

- 15 15. The method of Claim 14 wherein the first potential is ground potential.

16. A memory array substantially as hereinbefore described with reference to the accompanying drawings.

17. A method of accessing alternate word lines in a memory array substantially as hereinbefore described with reference to the accompanying drawings.

18. A method of preconditioning word lines in a memory array substantially as hereinbefore described with reference to the accompanying drawings.

Patents Act 1977

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(i) UK Cl (Edition K) G4C (C16C, C16X) G4A (AEF)

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Search Examiner

B J EDE

Databases (see over)

(i) UK Patent Office

(ii)

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Documents considered relevant following a search in respect of claims

1-5 AND 9-13

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
A	GB 2209858 A (NEC) - see Figure 2	1 and 9
A,P	EP 0424191 A2 (SUNDISK CORPORATION) - 24 APRIL 1991 - whole document relevant	1 and 9
X	EP 0198935 A1 (DEUTSCHE ITT) - whole document relevant	1 and 9
X	WO 84/01236 A1 (MOTOROLA) - whole document relevant	1 and 9
X	US 4817056 (K FURUTANI ET AL) - whole document relevant	1 and 9
A	US 4532611 (COUNTRYMAN) - whole document relevant	1 and 9

Category	Identity of document and relevant passages	Relevant to claim(s)

Categories of documents

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